100Gbps

QSFP28 AOC to 2x QSFP28 Breakout AOC

AC-D681-MFxxx-MMy

VERSION1
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www.cambridgeig.com

100Gbps QSFP28 to 2x 50G QSFP28 Breakout AOC
AC-D681-MFxxx-MMy

Features

- QSFP28 MSA Compliant
- Four-channel full-duplex channels
- Typical data rate up to 25.78125Gbps per channel
- Up to 100m on OM4 Multimode Fiber (MMF)
- Low power consumption <2.5W each terminal
- Operating case temperature -5°C to +70°C
- 4x25G electrical interface (OIF CEI-28G-VSR)
- 2x25G electrical interface (OIF CEI-28G-VSR)
- 3.3V power supply voltage
- RoHS 6 compliant
- Hot Pluggable QSFP form factor
- Built-in digital diagnostic function

Applications

- 100G Ethernet
- Infiniband EDR interconnects

Description

AC-D681-MFxxx-MMy is a high data rate parallel active optical cable for 100G Ethernet Applications. The AOC is terminated with 1x QSFP28 module at one end and 2x QSFP28 modules at the other. With the QSFP28 terminal, it offers 2 or 4 independent transmit and receive channels, each capable of 25.78125Gbps operation for an aggregate data rate of 103Gbps. These modules are designed to operate over multimode fiber systems using 850nm VCSEL laser and PIN to support the ultra-fast computing data exchange optical/electrical connection according to the QSFP Multi- Source Agreement (MSA).

It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

As per MSA specifications the module offers 7 low speed hardware control pins (including

Fiber length

The default fiber length of 100G QSFP28 AOC is 1 meter, but the fiber length of all kinds of AOC can be customized by different customer in the different applications.

Specification

Absolute Maximum Ratings						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Storage Temperature	TSTG	-40	-	+85	ºC	
Supply Voltage	Vcc3	-0.3		3.6	V	
Operating Relative Humidity	RH	0	-	+85	%	

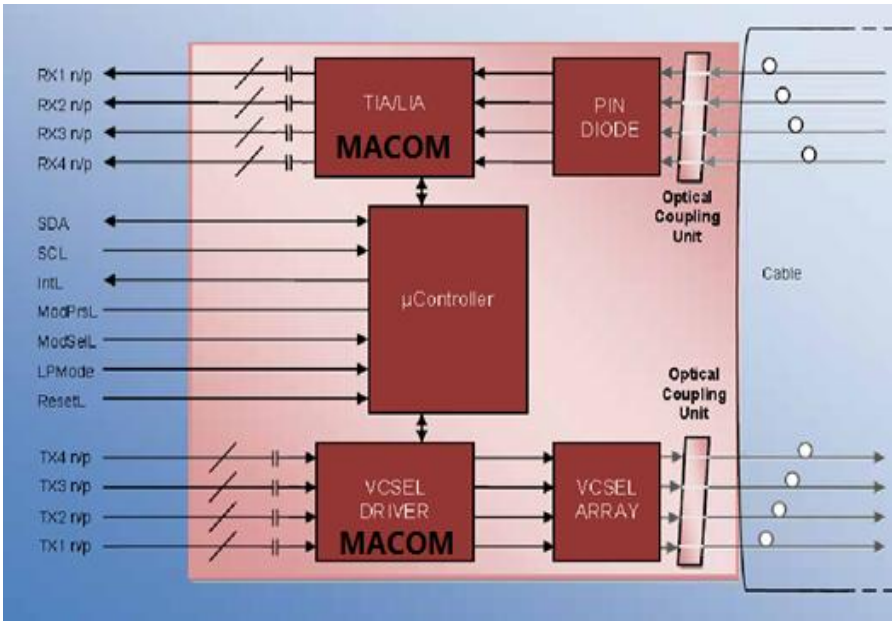
Recommended Operating Conditions						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Operating Case temperature	Ta	0	-	+70	ºC	
Supply Voltage	Vcc3	3.13	3.3	3.47	V	
Power Consumption (1x QSFP28)				2.5	W	1
Power Consumption (2x QSFP28)				2	W	1
Data Rate, each lane(1x QSFP28)			25.78125		Gbps	
Data Rate, each lane(2x QSFP28)			25.78125		Gbps	
Link Distance with OM3 Fiber		0	-	100	m	
Data Speed Tolerance	ΔDR	-100		+100	ppm	
Input Voltage High		2		VCC	V	
Input Voltage Low		0	-	0.8	V	

Electrical Specifications						
QSFP28 Transmitter (each Lane)						
Para meter	**Test Point**	**Min**	**Typical**	**Max**	**Units**	**Notes**
Overload Differential Voltage pk-pk	TP1a	900			mV	
Common Mode Voltage (Vcm)	TP1	-350		2850	mV	2
Differential Termination Resistance Mismatch	TP1			10	%	At 1MHz

Differential Return Loss (SDD11)	TP1			See CEI- 28G-VSR Equation 13-19	dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC11, SCD11)	TP1			See CEI- 28G-VSR Equation 13-20	dB	
Stressed Input Test	TP1a	See CEI-28G-VSR Section 13.3.11.2.1				
Receiver (each lane)						
Differential Voltage,pk-pk	TP4			900	mV	
Differential Voltage, pk-pk	TP4			900	mV	
Common Mode Voltage (Vcm)	TP4	-350		2850	mV	2
Common Mode Noise, RMS	TP4			17.5	mV	
Differential Termination Resistance Mismatch	TP4			10	%	At 1MHz
Differential Return Loss (SDD22)	TP4			See CEI- 28G-VSR Equation 13-19	dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC22, SCD22)	TP4			See CEI- 28G-VSR Equation 13-21	dB	
Common Mode Return Loss (SCC22)	TP4			-2	dB	3
Transition Time, 20 to 80%	TP4	9.5			ps	
Vertical Eye Closure (VEC)	TP4			5.5	dB	
Eye Width at 10-15 probability (EW15)	TP4	0.57			UI	
Eye Height at 10-15 probability (EH15)	TP4	228			mV	

Notes:
[1] per terminal
[2] Vcm is generated by the host. Specification inclides effects of ground offset voltage.
[3] From 250MHz to 30GHz

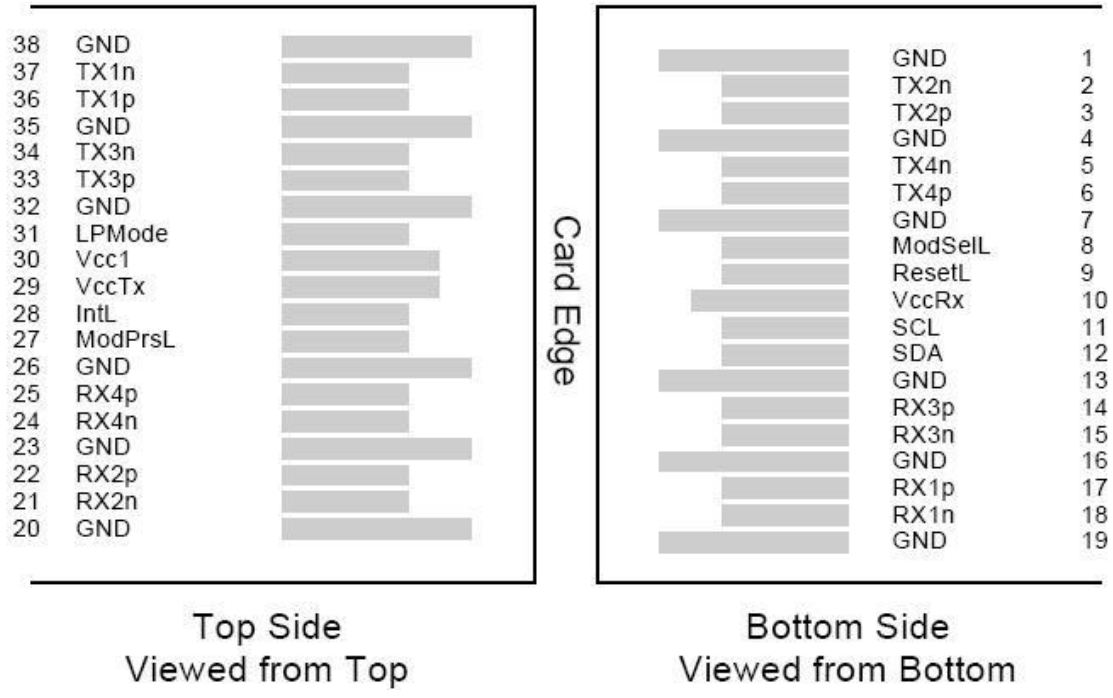
AOC Block Diagram



Block Diagram of the QSFP28 End Modules with MACOM solution

Figure1

Pin Diagram of QSFP28 Terminal



Pin-out Definition of QSFP28 Terminal

Pin	Logic	Name	1. Description	2. Note
1	GND	GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4	GND	GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7	GND	GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10	VccRx	VccRx	+ 3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	
30		Vcc1	+3.3 V Power Supply	

31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Notes:
[1] Module circuit ground is isolated from module chassis ground within the module.

1x or 2x QSFP28 Terminal

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP28 modules on a single 2-wire interface bus. When the ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host.
ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_ Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

The QSFP28 SR4 operates in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to VCC on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and will be deasserted “High” when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a critical status to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to VCC on the host board.

GND

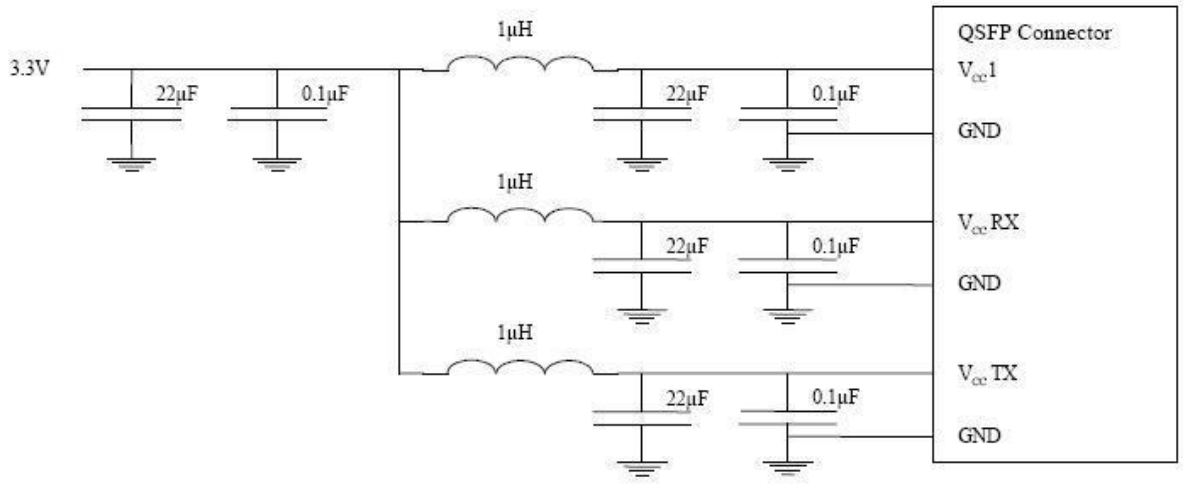
GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

VCC

VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 3 below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure2



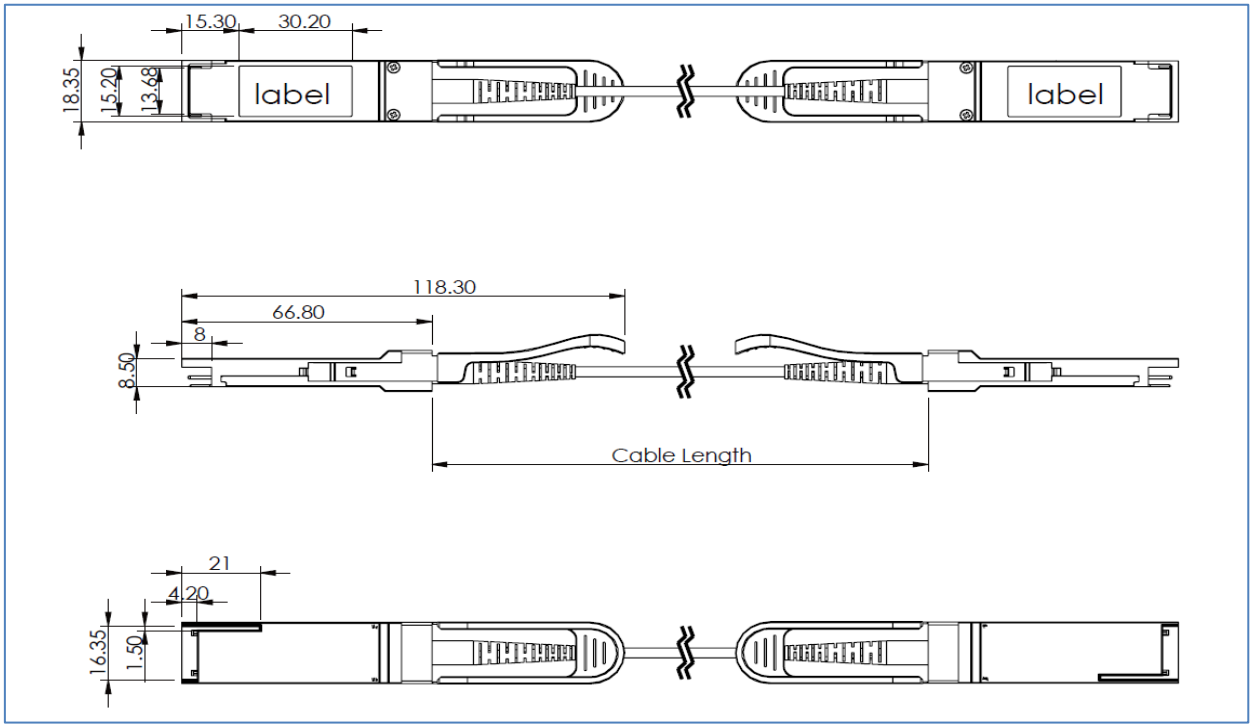
.Figure2. Host Board Power Supply Filtering

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all Cambridge QSFP28 AOC (Tx power monitor DDM function per customer request). A 2-wire serial interface provides user to contact with module. The structure of the memory is shown in Figure 5. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3		+3	degC	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	-0.1		0.1	V	Full operating range
Channel RX power monitor absolute error	DMI_RX	-3	-	3	Db	Per channel
Channel Bias current monitor	DMI_Ibias	-10%		10%	mA	Per channel
Channel TX power monitor absolute error	DMI_TX	-3	-	3	Db	Per channel

Dimensions



Ordering Information

1. P/N: AC-D681-MFxxx-MMy
2. XXX
   - XXX is length of fiber cable, in digital or letter. For exact number in meter, uses length number directly.

     For decimal number, uses “p”.

Length	Xxx
100m	100
10m	010
5m	005
1.5m	1p5
0.5m	0p5

3. Y
   - Y indicates color.

     0: orange, 1: Black, 2: Beige, 3: Blue, 4: Aqua

Part No.	Specification					
	Pack	Ttpical Rate	Tx	Rx	Top	Fiber length
AC-D681-MF001-Mmy	QSFP28 to QSFP28	103G	850nm VCSEL	PIN	0～70℃	1M
AC-D681-MF1P5-Mmy	QSFP28 to QSFP28	103G	850nm VCSEL	PIN	0～70℃	1.5M
AC-D681-MF002-Mmy	QSFP28 to QSFP28	103G	850nm VCSEL	PIN	0～70℃	2M
AC-D681-MF2P5-Mmy	QSFP28 to QSFP28	103G	850nm VCSEL	PIN	0～70℃	2.5M
AC-D681-MF003-MMy	QSFP28 to QSFP28	103G	850nm VCSEL	PIN	0～70℃	3M
AC-D681-MF3P5-MMy	QSFP28 to QSFP28	103G	850nm VCSEL	PIN	0～70℃	3.5M
AC-D681-MF004-MMy	QSFP28 to QSFP28	103G	850nm VCSEL	PIN	0～70℃	4M
AC-D681-MF4P5-MMy	QSFP28 to QSFP28	103G	850nm VCSEL	PIN	0～70℃	4.5M
AC-D681-MF005-MMy	QSFP28 to QSFP28	103G	850nm VCSEL	PIN	0～70℃	5M
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AC-D681-MF010-Mmy	QSFP28 to QSFP28	103G	850nm VCSEL	PIN	0～70℃	10M
AC-D681-MF020-MMy	QSFP28 to QSFP28	103G	850nm VCSEL	PIN	0～70℃	20M
AC-D681-MF025-MMy	QSFP28 to QSFP28	103G	850nm VCSEL	PIN	0～70℃	25M
AC-D681-MF030-MMy	QSFP28 to QSFP28	103G	850nm VCSEL	PIN	0～70℃	30M
AC-D681-MF090-MMy	QSFP28 to QSFP28	103G	850nm VCSEL	PIN	0～70℃	90M
AC-D681-MF099-MMy	QSFP28 to QSFP28	103G	850nm VCSEL	PIN	0～70℃	99M
AC-D681-MF100-MMy	QSFP28 to SFP+	103G	850nm VCSEL	PIN	0～70℃	100M

WARNING

Handling Precautions: This device is easy to be damaged as a result of ESD.A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.