# 100Gbps

## QSFP28 LR4 Transceivers

TR-D661-DF1M-OOA1

VERSION1

Feb. 2017


**www.cambridgeig.com**



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## Description

TR-D661-DF1M-OOA1 is a Four-Channel, Pluggable, Parallel, Fiber-Optic QSFP28 LAN-WDM4 Transceiver for InfiniBand EDR/FDR/QDR/DDR/SDR, 28G/14G/10G/8G/4G fiber channels, PCIE and SAS Applications. The data is transmitted bi-directionally with aggregate bandwidth of 100Gbps by four coarse WDM wavelengths normally at 1295nm, 1300nm, 1304nm, and 1309nm.The QSFP full-duplex optical module offers 4 independent transmit and receive channels. The optical transceiver module utilizes the optical engine designs and System in Package (SIP) integration technology, altogether with selected high quality DBF laser and PIN PDs to achieve reliable packet communication within data center.

## Features

- Compliant to IEEE 802.3bm electrical specifications
- Compliant to QSFP28 MSA Specifications
- Four-channel full-duplex transceiver modules
- Up to 10km link length over single mode fiber at 100Gbps
- Low power consumption: Max. 3.5W
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- 4x26Gb/s DFB-based LAN-WDM Transmitter
- RoHS 6 compliant
- Hot Pluggable QSFP form factor
- Duplex LC receptacles
- Built-in digital diagnostic function
- I²C Management Interface



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## Applications

- 100GBASE-LR4 100G Ethernet
- Proprietary Interconnections
- Infiniband 4X SDR DDR QDR

## Specification

**Absolute Maximum Ratings**

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Storage Temperature | $T_{STG}$ | -40 | - | +85 | ºC | |
| Supply Voltage | Vcc3 | -0.3 | | 3.6 | V | |
| Operating Relative Humidity | RH | 0 | - | +85 | % | |

**Recommended Operating Conditions**

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Operating Case temperature | Ta | 0 | - | +70 | ºC | |
| Supply Voltage | $V_{CC3}$ | 3.13 | 3.3 | 3.47 | V | |
| Power Consumption | | | | 1.5 | W | |
| Data Rate | | | 25.78125 | | Gbps | |
| Link Distance with SM Fiber | | 0 | 2 | - | Km | |
| Data Speed Tolerance | ΔDR | -100 | | +100 | ppm | |

**Transmitter Operating Characteristic-Optical, Electrical**

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Centre Wavelength Ch0 | $\lambda_C$ | 1294.53 | | 1296.59 | nm | Note1 |
| Centre Wavelength Ch1 | | 1299.02 | | 1301.09 | | |
| Centre Wavelength Ch2 | | 1303.54 | | 1305.63 | | |
| Centre Wavelength Ch3 | | 1308. | | 1310.1 | | |



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| | | | | | | |
|---|---|---|---|---|---|---|
| | | 09 | | 9 | | |
| Average Optical Power, each Lane | Pavg | -1.3 | - | 4.5 | dBm | |
| Average Launch Power OFF Transmitter, each Lane | Poff | - | - | -30 | dBm | |
| Optical Modulation Amplitude (OMA), each Lane | Poma | -1.0 | - | 4.5 | dBm | Note1 |
| Optical Return Loss Tolerance | RL | - | - | 20 | dB | |
| Transmitter Reflectance | RT | - | - | -12 | dB | |
| Extinction Ratio | ER | 4.0 | - | | dB | |
| Rise/Fall Time , 20%~80% | Tr/Tf | | - | 12 | Ps | |
| Side mode Suppression ratio | SSR | 30 | - | - | dB | |
| Transmitter Eye Mask Margin | EMM | 10 | 20 | - | % | Note2 |
| Transmitter Eye Width | | - | 0.46 | - | UI | |
| Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3} | {0.25, 0.4, 0.45, 0.25, 0.28, 0.4} | | | | | |

**Notes:**

[1] Transmitter wavelength, RMS spectral width and power need to meet the OMA minus TDP specs to guarantee link performance

[2] The eye diagram is tested with 1000 waveform

**Receiver Operating Characteristic-Optical, Electrical**

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Centre Wavelength Ch0 | λc | 1294.53 | | 1296.59 | nm | Note1 |
| Centre Wavelength Ch1 | | 1299.02 | | 1301.09 | | |
| Centre Wavelength Ch2 | | 1303.54 | | 1305.63 | | |
| Centre Wavelength Ch3 | | 1308.09 | | 1310.19 | | |
| Signaling Speed per Lane | | | 25.78125 | | Gb/s | Note1 |
| Receive Sensitivity in OMA, each Lane | SEN | - | - | -8.6 | dBm | Note2 |
| Damage Threshold | THd | +3 | - | | dBm | |
| Stressed Receiver Sensitivity in OMA, each Lane | SRS | - | - | -6.8 | dBm | |
| Los Assert | LOSA | -24 | - | -13.6 | dBm | |
| Los Dessert | LOSD | | - | -11.6 | dBm | |



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| | | | | | | |
|---|---|---|---|---|---|---|
| Los Hysteresis | LOSH | 0.5 | 1.5 | - | dB | |
| Overload each Lane | OVL | +2.4 | - | | dBm | |
| Receiver Reflectance | | - | - | -12 | dB | |

**Notes:**

[1] Receiver consists of 4 photodetectors operating at a maximum rate of 25.78Gb/s each

[2] Receiver sensitivity is informative. Stressed receiver sensitivity shall be measured with conformance test signal for BER =5x $10^{-5}$

**Electrical Specifications**

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Differential input impedance | Zin | 90 | 100 | 110 | ohm | |
| Differential Output impedance | Zout | 90 | 100 | 110 | ohm | |
| Differential input voltage amplitude | ΔVin | 300 | | 2800 | mVp-p | |
| Differential output voltage amplitude | ΔVout | 400 | | 800 | mVp-p | |
| Input Logic Level High | VIH | 2.0 | | VCC | V | |
| Input Logic Level Low | VIL | 0 | | 0.8 | V | |
| Output Logic Level High | VOH | VCC-0.5 | | VCC | V | |
| Output Logic Level Low | VOH | 0 | | 0.4 | V | |
| Bit Error Rate | BR | 0 | | 5 x $10^{-5}$ | | |



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## Pin Diagram

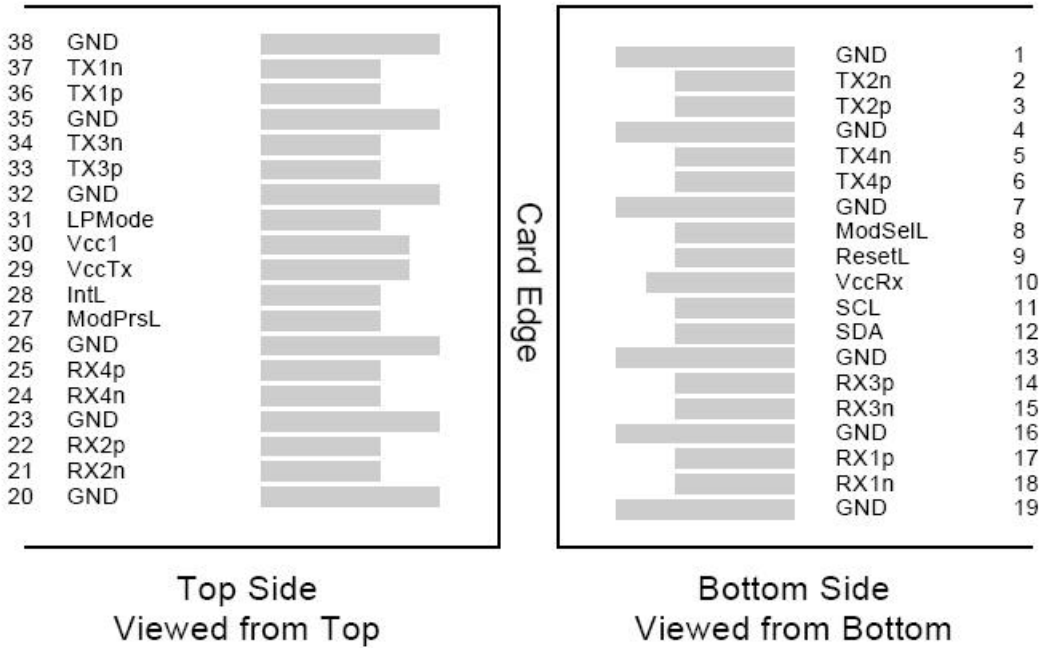


Figure1

## Pin-out Definition

| Pin | Logic | Name | Description | Note |
|---|---|---|---|---|
| 1 | GND | GND | Ground | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data output | |
| 4 | GND | GND | Ground | 1 |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input | |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data output | |
| 7 | GND | GND | Ground | 1 |
| 8 | LVTLL-I | ModSelL | Module Select | |
| 9 | LVTLL-I | ResetL | Module Reset | |



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| | | | | |
|---|---|---|---|---|
| 10 | VccRx | VccRx | + 3.3V Power Supply Receiver | 2 |
| 11 | LVCMOS-I/O | SCL | 2-Wire Serial Interface Clock | |
| 12 | LVCMOS-I/O | SDA | 2-Wire Serial Interface Data | |
| 13 | | GND | Ground | |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output | |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output | |
| 16 | | GND | Ground | 1 |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | |
| 19 | | GND | Ground | 1 |
| 20 | | GND | Ground | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | |
| 23 | | GND | Ground | 1 |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | 1 |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | |
| 26 | | GND | Ground | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present | |
| 28 | LVTTL-O | IntL | Interrupt | |
| 29 | | VccTx | +3.3 V Power Supply transmitter | |
| 30 | | Vcc1 | +3.3 V Power Supply | |
| 31 | LVTTL-I | LPMode | Low Power Mode | |
| 32 | | GND | Ground | 1 |
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input | |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Output | |
| 35 | | GND | Ground | 1 |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input | |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Output | |
| 38 | | GND | Ground | 1 |

**Notes:**

[1] Module circuit ground is isolated from module chassis ground within the module. GND is the symbol for signal and supply (power) common for QSFP28 modules.



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## ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP28 modules on a single 2-wire interface bus. When the ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host.

ModSelL has an internal pull-up in the module.

## ResetL Pin

Reset. LPMode_ Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset

## LPMode Pin

The QSFP28 CR4 operates in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.



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## ModPrsL Pin

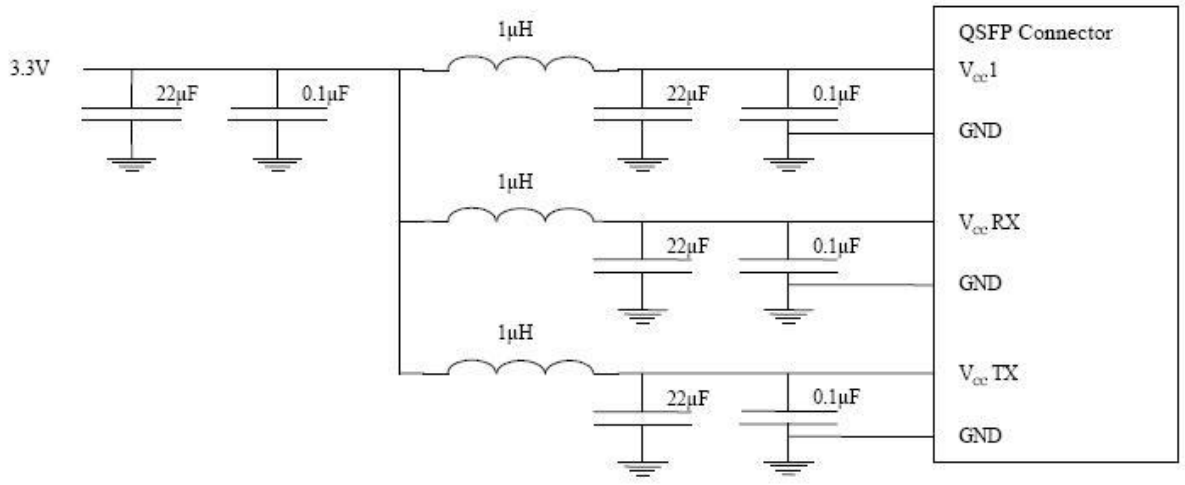
ModPrsL is pulled up to VCC on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and will be deasserted “High” when the module is physically absent from the host connector.

## IntL Pin

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a critical status to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to VCC on the host board.

## Power Supply Filtering

The host board should use the power supply filtering shown in Figure2




.Figure2. Host Board Power Supply Filtering



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## DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all Cambridge QSFP28 LR4 (Tx power monitor DDM function per customer request). A 2-wire serial interface provides user to contact with module. The structure of the memory is shown in Figure 5. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Temperature monitor absolute error | DMI_Temp | -3 | | +3 | degC | Over operating temp |
| Supply voltage monitor absolute error | DMI _VCC | -0.1 | | 0.1 | V | Full operating range |
| Channel RX power monitor absolute error | DMI_RX | -3 | - | 3 | db | Per channel |
| Channel Bias current monitor | DMI_Ibias | -10% | | 10% | mA | Per channel |
| Channel TX power monitor absolute error | DMI_TX | -3 | - | 3 | db | Per channel |



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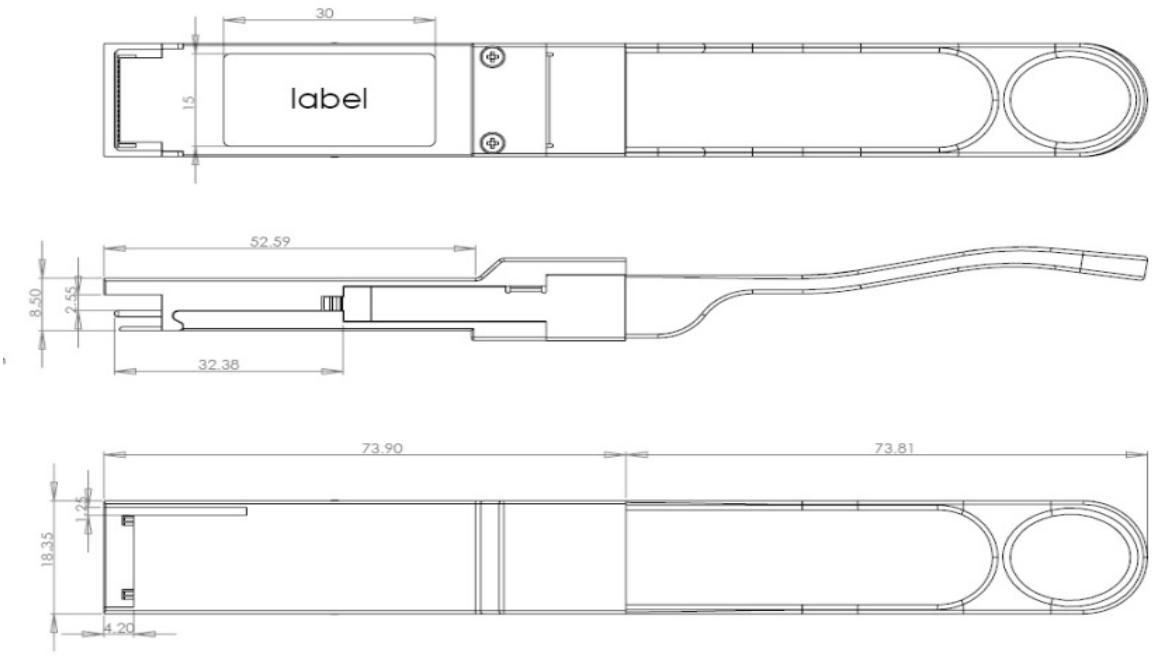
## Dimensions




## Ordering Information

| Part No. | Specification | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Pack | Rate | Tx | Pout | Rx | S | Top | Reach |
| TR-D661-DF1M-00A1 | QSFP28 | 100G | LWDM DFB | -1.3 ~ 4.5dBm | PIN | ＜-8.6dBm | 0～70℃ | 10Km |

## WARNING

Handling Precautions: This device is easy to be damaged as a result of ESD. A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.



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